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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Bailey et al.

Application No. 09/883,836

Filed: June 17, 2001

Confirmation No. 9966

For: COHERENT STATE AMONG MULTIPLE  
SIMULATION MODELS IN AN EDA  
SIMULATION ENVIRONMENT

Examiner:

Art Unit: 2123

Attorney Reference No. 1011-64537-01

CERTIFICATE OF MAILING

I hereby certify that this paper and the documents referred to as being attached or enclosed herewith are being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450 on the date shown below.

Attorney  
for Applicants

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Listed on the accompanying form PTO-1449 and enclosed herewith are several English-language documents. Applicants respectfully request that these documents be listed as references cited on the issued patent.

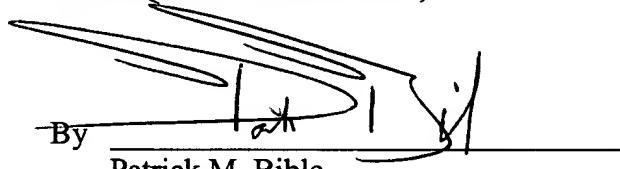
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The filing of this IDS shall not be construed to be an admission that the information cited in the statement is, or is considered to be, prior art or otherwise material to patentability as defined in 37 C.F.R. §1.56.

Respectfully submitted,

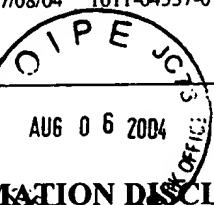
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AUG 06 2004

**INFORMATION DISCLOSURE STATEMENT  
BY APPLICANT**

Attorney Docket Number	1011-64537-01
Application Number	09/883,836
Filing Date	June 17, 2001
First Named Inventor	Bailey
Art Unit	2123
Examiner Name	

**U.S. PATENT DOCUMENTS**

NOTE: If this application was filed after June 30, 2003, copies of United States patents and United States published patent applications do not have to be provided to the Patent Office. This requirement of 37 C.F.R. § 1.98(a)(2)(i) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on August 5, 2003 (1276 OG 55).

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
		5,768,567	6.16.1998	Klein et al.

**FOREIGN PATENT DOCUMENTS**

Examiner's Initials*	Cite No. (optional)	Country	Number	Publication Date	Name of Applicant or Patentee
		Europe	EP 0 418 980	3.27.1991	

**OTHER DOCUMENTS**

	Harris et al., "The co-verification of an RTOS in an SOC," <i>Integrated System Design</i> , CMP Media Inc., USA, Vol. 13, No. 143, pp. 23-30 (May 2001).
	Shah et al., "Target processor and co-verification environment independent adapter--a technology to shorten cycle-time for retargeting TI processor simulators in HW/SW co-verification environments," ASIC/SOC Conference Proceedings, pp. 37-41 (September 1999).
	Yoo et al., "Fast hardware-software coverification by optimistic execution of real processor," Proceedings Design, Automation and Test in Europe Conference and Exhibition 2000, Proceedings of Meeting on Design Automation and Test in Europe, Paris, France, pp. 663-668 (March 2000).

EXAMINER SIGNATURE:	DATE CONSIDERED:
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\* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.